Advanced Amorphous Silicon Thin-Film Transistors for AM-OLEDs: Electrical Performance and Stability

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***Abstract*—We fabricated and characterized the advanced amorphous silicon thin-film transistors with a bilayer structure for both the active and gate dielectric films. The electrical field across the gate insulator has a significant influence on the device threshold voltage electrical stability. We show that high thin-film transistor stability can be achieved even under the presence of a high channel current. Its electrical and high-temperature stability improves up to a factor of five when the TFT biasing condition changes from the linear to the saturation region of operation.**

***Index Terms*—Advanced amorphous silicon thin-film transistor (a-Si:H TFT), bias temperature stress (BTS), biasing condition, circuit stability, current temperature stress (CTS).**

I. Introduction

THE HYDROGENATED amorphous silicon thin-film transistor (a-Si:H TFT) has been a desirable choice in the flat-panel display industry for more than two decades [1], [2]. The utilization of the a-Si:H technology in the active-matrix liquid crystal displays (AM-LCD) and the active-matrix organic light emitting displays (AM-OLEDs) requires transistors that exhibit high mobility and low threshold voltage values, and with a high production throughput [3]. These qualities make possible the production of large-size displays with low power consumption at relatively low costs. The electrical performance of the a-Si:H TFT is intimately related to the electronic quality of the a-Si:H film, and, in general, a high-quality film can only be fabricated at low deposition rates [4]. Similarly, the deposition rate of the amorphous silicon nitride (a-SiN_X:H) gatex insulator must also be low to achieve a high-quality a-SiN_X:H/a-Si:H interface. A high-quality interface is necessary in producing a transistor with a low threshold voltage and a subthreshold swing, and for achieving high electrical stability [5]. This insulating layer should exceed 4000 Å to reduce the gate leakage.

Unfortunately, the use of low deposition rates in fabricating high-performance TFTs reduces the overall device production throughput due to longer deposition times. It is, therefore, desirable to strike a compromise between a transistor's electrical performance and the overall production throughput by depositing the a-SiN_X:H and a-Si:H films at reasonably high rates without significantly degrading the overall a-Si:H TFT electrical characteristics. One possible solution is to deposit the TFT active layer in two successive steps—a low-deposition-rate film near the a-SiN_X:H/a-Si:H interface to achieve a high-electronic-quality a-Si:H film near the electron conduction channel, and a high-deposition-rate film in the back channel to provide an etching buffer. The a-SiN_X:H deposition can also be separated into a two-step process—a low-deposition-rate film near the high-quality a-Si:H film for optimal electrical performance, and a high-deposition-rate film near the gate metal to reduce the gate leakage [6]. This advanced a-Si:H TFT shows acceptable electrical performance while maintaining a sufficiently high production throughput to be useful in the commercial applications.

It is well known that the traditional a-Si:H TFTs suffer from electrical degradation, namely, the positive-direction threshold voltage shift ΔV_T, which can cause nonuniformity in TFT threshold voltages across the AM-OLED. This, in turn, lowers the luminance of individual pixels over time, causing display nonuniformity [7]–[11]. The advanced a-Si:H TFT is not immune from these deleterious effects, thus necessitating a thorough study of the mechanics of these device stability issues.

The positive threshold voltage shift phenomenon is due to the trapping of electrons in the hydrogenated amorphous silicon nitride gate insulator (a-SiN_X:H) [12], [13] and near the a-SiN_X:H/a-Si:H interface [14], [15], the creation of metastable states in the amorphous silicon [16], [17], or a combination of both mechanisms [18], [19]. This type of threshold voltage shift appears to be larger at elevated temperatures because both trapping of electrons and states creation are thermally activated processes [14]. Incidentally, in an AM-OLED, joule heating from the organic light-emitting diodes can reach up to 86 °C during its operation [20], which means that the temperature inside an AM-OLED can reach a comparable level. Thus, transistors in an AM-OLED may operate under an elevated temperature, where the threshold voltage degradation mechanisms mentioned above are accelerated. An increase in the threshold voltage leads to a decrease in the drain current if both gate and drain voltages remain the same on a given transistor. A positive threshold voltage shift of the driving transistors in a pixel electrode circuit of an AM-OLED can lower the OLED's luminance [21]–[23] since it is proportional to the current provided by the a-Si:H driving transistor [24]. This degradation negatively impacts the viewing quality of the AM-OLED.

In this paper, we examine the advanced a-Si:H TFTs' electrical characteristics, as well as their threshold voltage stability under the extended application of current and voltage stresses at an elevated temperature. We combine the experimental results

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from our TFT stability measurements with a computational simulation to quantify the effect of the TFT threshold voltage shift on the overall performance of an AM-OLED pixel electrode circuit. To our best knowledge, this is the first comprehensive investigation on the electrical performance and stability of the advanced a-Si:H TFTs and their impact on the degradation of flat-panel displays.

II. Experimental

The fabrication process for the advanced a-Si:H TFTs has been described elsewhere [6]. All electrical measurements were carried out in a Karl Suss probe station. The device temperature was regulated by means of a heated chuck and a Signatone temperature controller with a precision of 0.1 K. Electrical characteristics were measured using an HP 4156A Parameter Analyzer via the Metrics Interactive Control Software on a computer. We measured both the linear ($V_{\rm DS} < V_{\rm GS} - V_T$) and the saturation ($V_{\rm D-SAT} > V_{\rm GS} - V_T$) region transfer characteristics of the advanced a-Si:H TFT at measurement temperatures ($T_{\rm MEAS}$) ranging from 293 to 353 K; $V_{\rm DS}$, $V_{\rm D-SAT}$, $V_{\rm GS}$, and V_T denote the drain, saturation drain, gate, and threshold voltages, respectively. Prior to the measurement, all TFTs were annealed at 473 K for 1 h in nitrogen. The chuck was first heated to the desired $T_{\rm MEAS}$ before the advanced a-Si:H TFTs were placed on top of it. We allowed a 10-min stabilization time before the electrical measurement to avoid recording artifacts from thermal shock. For the electrical measurement of the TFT's transfer characteristics operating in the linear region, the parameter analyzer internally grounded the source terminal, applied a constant voltage of 0.1 V on the drain terminal, and swept the voltage on the gate terminal from -10 to 20 V with a 0.1-V interval. For the saturation region transfer characteristics, the setup was identical to that of the linear regime except that the analyzer internally synchronized the drain and gate terminals to the same bias instead of applying a constant bias on the drain terminal. The currents flowing into the drain, the gate, and the sources were collected by the parameter analyzer, with currents flowing into the terminals denoted as the positive direction. Throughout the measurement of the electrical characteristics, the TFT remained at $T_{\rm MEAS}$, with a fluctuation of less than 0.1 K. Each transistor was measured only once at $T_{\rm MEAS}$ to avoid electrical and thermal stresses.

We also study the effects of prolonged application of bias stresses at an elevated temperature of 353 K ($T_{\rm STR}$). During the bias temperature stress (BTS) experiments, constant biases were continuously applied to the gate, the drain, and/or the source of the TFTs. At the specified intervals, the biases were suspended for less than 10 s to measure the saturation transfer characteristics of the transistors at the same temperature, or $T_{\rm MEAS} = T_{\rm STR}$. The duration of the electrical stress applied to the TFT is denoted as the stressing time $t_{\rm STR}$. We acknowledge that there will be some unwanted errors from this style of measurement. First, the interruption of the bias stress to measure the transfer characteristics allows the restoration of charges, and, second, the application of voltages when taking the drain current versus gate-to-source voltage (I_D–$V_{\rm GS}$) characteristics can add an additional stress to the a-Si:H TFT. However,

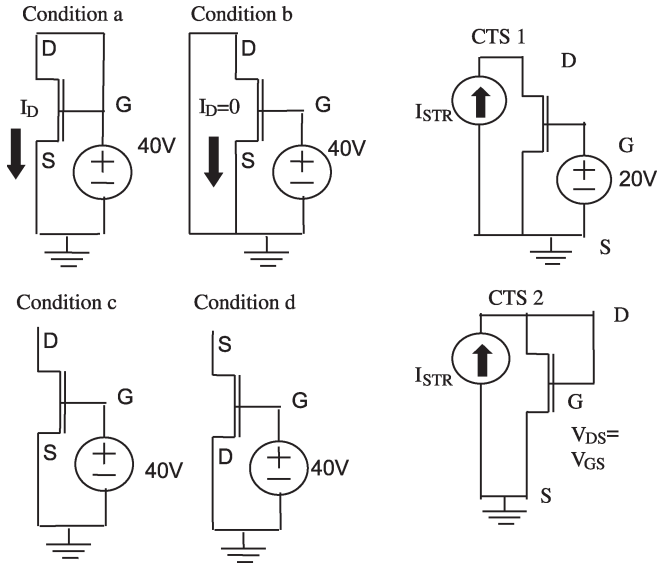

Fig. 1. (Left) BTS experimental setups for four a-Si:H TFT stressing conditions described in the text, and (right) CTS experimental setups used in this paper: CTS 1 ($V_{\rm GS} = 20$ V) and CTS 2 ($V_{\rm GS} = V_{\rm DS}$). The stress current $I_{\rm STR}$ levels are 10 nA, 500 nA, and 5.5 μA.

contributions from both factors should not significantly skew the degradation behavior over a long period of time, as both the interruption and the measurement last only a few seconds. Four BTS experiments were carried out with the following biasing conditions: a) $V_{\rm GS} = V_{\rm DS} = 40$ V; b) $V_{\rm GS} = 40$ V and $V_{\rm DS} = 0$ V; c) $V_{\rm GS} = 40$ V and the drain was floating; and d) $V_{\rm GD} = 40$ V and the source was floating (Fig. 1).

Current temperature stress (CTS) measurements were also performed. During the CTS experiment, a constant electrical current $I_{\rm STR}$ was applied to the drain of the advanced a-Si:H TFT at $T_{\rm STR} = 353$ K. There were two different TFT biasing schemes for the CTS experiments—CTS 1 and CTS 2. For CTS 1, the gate was biased at 20 V, whereas $I_{\rm STR}$ was applied to the drain of the TFT. For CTS 2, the gate and the drain were externally shorted together [$V_{\rm DS}(t) = V_{\rm GS}(t)$] during the CTS experiments, which meant that the $I_{\rm STR}$ going into the drain also set up the bias on the gate (Fig. 1). CTS 1 is equivalent to operating the TFT in the linear region, and CTS 2 operates in the saturation region. The measurement technique, the stress duration, and the measurement time intervals were the same as those of the BTS experiments. The stress current ranges from 10 nA to 5.5 μA. The stress currents reflect the current levels required to drive an OLED pixel of an XGA display [25].

It is important to emphasize that the BTS and the CTS are differently stressed over a long period of time. In the BTS, the biases at the gate, the drain, and the source are biased at constant voltages throughout the stressing experiment; this means that the band bending in the amorphous silicon reduces over time because of the electrons trapped near the a-Si:H/a-SiN$_X$:H interface. On the contrary, the gate and/or drain voltages in the CTS experiment increase over time to maintain the stressing current that would otherwise decrease due to the electrical stress-induced degradation (shift toward more positive $V_{\rm GS}$) of the a-Si:H TFT's characteristics. The increase in biasing voltages keeps the band bending in the a-Si:H constant. In the

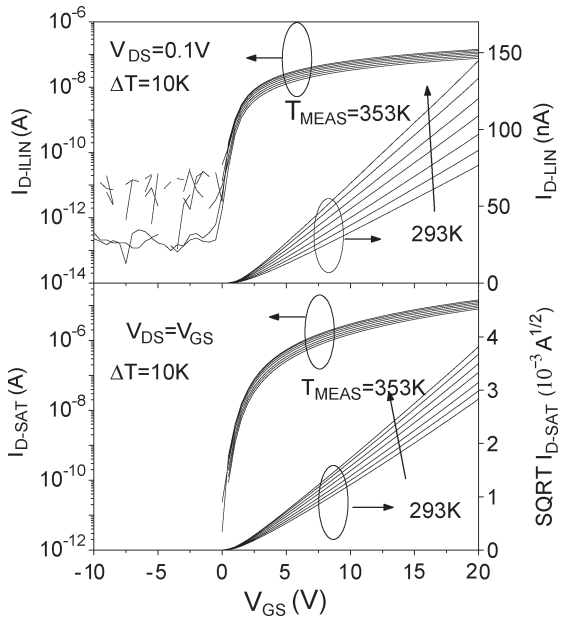

Fig. 2. Linear and saturation transfer characteristics of a-Si:H TFTs measured from $T_{\mathrm{MEAS}} = 293$ to 353 K.

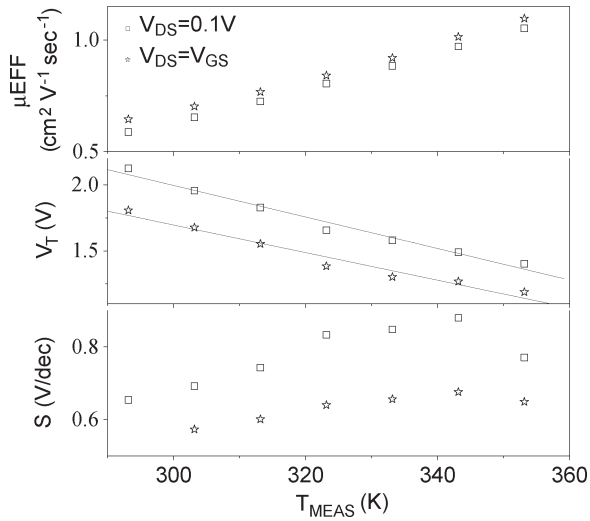

Fig. 3. Field-effect mobility, threshold voltage, and subthreshold swing change with the measurement temperature. Symbols represent experimental data, and lines are the numerical fit.

BTS experiment, the current decreases, and the bias remains constant, whereas in the CTS experiment, the bias increases, and the current remains the same. These discrepancies lead to difficulties when comparing results collected from BTS and CTS experiments.

III. Experimental Results and Discussion

A. Temperature Effect on the a-Si:H TFTs

From the transfer characteristics of the advanced a-Si:H TFT measured at different temperatures (Fig. 2), we extracted the field-effect mobility μ_{EFF}, the threshold voltage V_T, and the subthreshold swing S of the transistors (Fig. 3). Experimental data were fitted to the transistor square law equations based on the gradual channel approximation for the linear and saturation regions of operation to obtain μ_{EFF} and V_T [26], i.e.,

$$I_{\mathrm{D-LIN}} = \frac{W}{L}\mu_{\mathrm{EFF}}C_{\mathrm{INS}}\left(V_{\mathrm{GS}} - V_T - \frac{V_{\mathrm{DS}}}{2}\right)V_{\mathrm{DS}} \quad (1)$$

$$(I_{\mathrm{D\text{-}SAT}})^{1/2} = \left(\frac{W}{2L}\mu_{\mathrm{EFF}}C_{\mathrm{INS}}\right)^{1/2}(V_{\mathrm{GS}} - V_T). \quad (2)$$

Although the TFT transfer characteristics can deviate from ideal with nonlinear transfer characteristics (i.e., exponent of $V_{\mathrm{GS}} - V_T$ term is not 1), we use data range from 10% to 90% of I_D ($V_{\mathrm{GS}} = 20$ V) to compare different μ_{EFF} values [27]. If the exponent of $V_{\mathrm{GS}} - V_T$ changes with the temperature, μ_{EFF} will have different units ($\mathrm{cm}^2\ \mathrm{V}^{-\exp}\ \mathrm{s}^{-1}$ instead of $\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$) and can no longer be fairly evaluated. Our choice of using the 10%–90% data range is justified by the consistency of both the linear and saturation region transfer characteristic curvatures within this range. The mean exponents based on the nonlinear [27] fit are 1.061 with a standard deviation of 0.0007, and 1.068 with a standard deviation of 0.001, in the linear and saturation regions, respectively, for T_{MEAS} ranging from 293 to 353 K. The S values were extracted by selecting a set current value for each region of operation (0.1 nA for the linear region and 1 nA for the saturation region) as the center value and fitting a straight line to the three data points near the center value (the center value, plus one point above and below it). The inverse of the slope of the straight line is defined as the subthreshold swing value. This method defines S at a given current density level, which allows an unbiased comparison of the TFT characteristics at different T_{MEAS} [28]. Both μ_{EFF} and S increase with temperature, whereas V_T decreases with increasing temperature. Details of the physics dictating these behaviors have been addressed by numerous groups [17], [18], [29], [30]. Larger mobility at higher temperatures suggests that the transport of carriers obeys the multiple trapping model described by LeComber and Spear [31] as well as Tiedje *et al.* [32]. In the multiple trapping model, electrons at a high temperature (> 240 K) move through amorphous silicon by alternating between drifting along the extended states of the conduction band and residing in localized deep gap states; the transition between the two modes is due to the trap and thermal release, which causes the increase in the mobility at a higher temperature as the electrons escape from the deep traps more frequently. The relation between the mobility and the temperature in the multiple trapping model is exponential in nature and can be described by [29]–[32]

$$\mu = \mu_O \exp\left(-\frac{E_D}{kT_{\mathrm{MEAS}}}\right) \quad (3)$$

where μ_O is the mobility prefactor, and E_D is the electron mobility activation energy. Our TFT has E_D of 87.5 meV and μ_O of 18.67 $\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$ in the linear region and 81.1 meV and 15.70 $\mathrm{cm}^2 \cdot \mathrm{V}^{-1} \cdot \mathrm{s}^{-1}$ in the saturation region (Fig. 4, inset). Lustig *et al.* also attributed it to a decrease in the contact resistance at an elevated temperature.

The mobility activation energy signifies the energy difference between the edge of the conduction band E_C and the Fermi

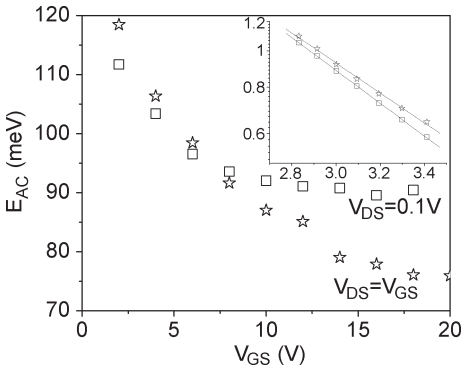

Fig. 4. Drain current activation energy variation with the gate voltage for the linear ($V_{\rm DS} = 0.1$ V) and saturation ($V_{\rm DS} = V_{\rm GS}$) regions of the device operation. The inset shows the field-effect mobility variation as a function of $1/T_{\rm MEAS}$ for the a-Si:H TFT used in this paper.

level E_F; it equates to the average energy that the trapped electrons need to gain to escape from the localized states and into the extended states [32], [33]. One note that we need to emphasize is that the temperature has the same effect on both the field effect and the drift mobility [34], which means that the temperature effect is intrinsic to the amorphous silicon and not dependent on the device geometry or the modes of operation. Temperature also has an effect on the transistor's contact resistance. Based on a simulation of the a-Si:H TFT with different source/drain contact resistance values, field-effect mobility increases from 0.6 to 1.1 $\rm cm^2 \cdot V^{-1} \cdot s^{-1}$ when the specific contact resistance decreases from 0.9 to 0.2 $\Omega \cdot \rm cm^2$ [35]. However, it is unlikely for the specific contact resistance to decrease by a factor of four with a temperature increase of 60 K. This leads us to conclude that, although the contact resistance may decrease with the increasing temperature, the primary cause for the observed mobility increase comes from the thermal activation of the electron transport within the device channel. The threshold voltage decreases with the increasing temperature because a lower surface potential is needed to release the trapped electrons in the bulk amorphous silicon from the localized states into the extended states at an elevated temperature [36]. Moreover, the surface state ionization at the a-SiN$_X$:H/a-Si:H interface also contributes to this decrease [37]. As free electrons from both ionization processes accumulate near the interface, the surface band bending increases, and the Fermi level at the interface moves closer toward the conduction band. The following linear equation is used to describe the threshold voltage dependence on the transistor operating temperature [29]:

$$V_T(T_{\rm MEAS}) = V_T(T_O) - \alpha(T_{\rm MEAS} - T_O) \tag{4}$$

where T_O is the room temperature in Kelvin, and α is an empirical parameter extracted from the experiment; for our devices, we obtain α values of 0.012 V/K for the linear region and 0.01 V/K for the saturation region and $V_T(T_O)$ values of 2.15 V for the linear region and 1.78 V for the saturation region. The ionization of both bulk and interface states is also responsible for the increase in the subthreshold swing with the temperature. More available states in both deep and shallow states at a higher temperature lead to a larger S value because the Fermi level sweeps at a slower rate due to the pinning of unoccupied states. By using the following equation for the maximum bulk $N_{\rm bs}$ and surface $N_{\rm ss}$ state densities calculation [38]:

$$S = \frac{kT_{\rm MEAS}}{q\log(e)}\left[1 + \frac{qx_i}{\varepsilon_i}\left(\sqrt{\varepsilon_s N_{\rm bs}} + qN_{ss}\right)\right] \tag{5}$$

we found that for $T_{\rm MEAS}$ of 293.15–343.15 K, $N_{\rm bs}$ changes from 1.4×10^{17} to 1.9×10^{17} $\rm cm^{-3} \cdot eV^{-1}$ for the linear region and from 9.8×10^{16} to 1.07×10^{17} $\rm cm^{-3} \cdot eV^{-1}$ for the saturation region when $N_{\rm ss}$ is assumed to be 0. Similarly, $N_{\rm ss}$ in the same $T_{\rm MEAS}$ range changes from 9.63×10^{11} to 1.12×10^{12} $\rm cm^{-2} \cdot eV^{-1}$ for the linear region and from 8.01×10^{11} to 8.38×10^{11} $\rm cm^{-2} \cdot eV^{-1}$ for the saturation region when $N_{\rm bs}$ is assumed to be 0. In this equation, ε_i and ε_s are the a-SiN$_X$:H and a-Si:H dielectric constants, respectively. Although this calculation does not separate the bulk and surface states when calculating the subthreshold swing value, we see that both can increase with the operating temperature of the transistor.

We extracted the drain current activation energy ($E_{\rm AC}$) at different gate biases following the method described by Lustig *et al.* [30], Lustig and Kanicki [39], and Chen and Kanicki [40], and the resulting activation energies for different $V_{\rm GS}$ values are shown in Fig. 4. The drain current activation energy decreases from 112 to 90 meV in the linear region and from 120 to 75 meV in the saturation region when $V_{\rm GS}$ increases from 2 to 20 V. This trend is consistent with the results reported by Lustig *et al.*, Lustig and Kanicki, and Chen and Kanicki, but the range is lower—their drain current activation energy values decrease from about 500 to 50 meV as $V_{\rm GS}$ increases from 2 to 20 V for both linear and saturation regions. This activation energy represents the average energy required for the electrons to escape from the less mobile deep trap states into the more mobile band tail states [37]. Naturally, as band bending increases, as a result of the application of the gate voltage, this energy decreases because the Fermi level moves closer to the edge of the conduction band tail states. More importantly, the range of the $E_{\rm AC}$ value is indicative of the electronic quality of the amorphous silicon. For a steep conduction band tail slope, the Fermi level lies closer to the conduction band edge due to the less pinning effect, which results in a smaller $E_{\rm AC}$. On the contrary, lower electronic quality amorphous silicon will have a higher range of values of activation energy. Chen [35] computed the a-Si:H TFT drain current activation energy values for the gate voltage ranging from 0 to 20 V with different conduction band tail slope values. Based on his simulation results [35], our amorphous silicon has a conduction band tail slope of around 28 ± 3 meV.

The dual a-Si:H and a-SiN$_X$:H layer TFT shows promising linear region electrical performance with field-effect mobility of 0.6 $\rm cm^2 \cdot V^{-1} \cdot s^{-1}$, a threshold voltage of 2.1 V, and a subthreshold swing of 0.65 V/dec at room temperature, and field-effect mobility of 1.1 $\rm cm^2 \cdot V^{-1} \cdot s^{-1}$, a threshold voltage of 1.4 V, and a subthreshold swing of 0.77 V/dec at 353 K. The drain current activation energy decreases from 120 to 90 meV as $V_{\rm GS}$ increases from 2 to 20 V. The conduction band tail slope is around 28 meV. Compared to the state-of-the-art a-Si:H TFT with the active and gate insulator layers deposited

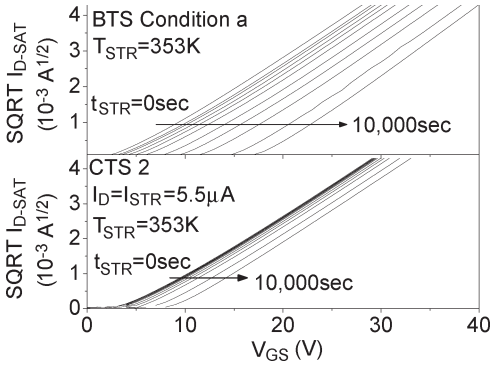

Fig. 5. Examples of $I_{\mathrm{D-SAT}}^{1/2}$ versus V_{GS} characteristics of the a-Si:H TFTs in the saturation region of operation measured for the (top) BTS and (bottom) CTS experiments.

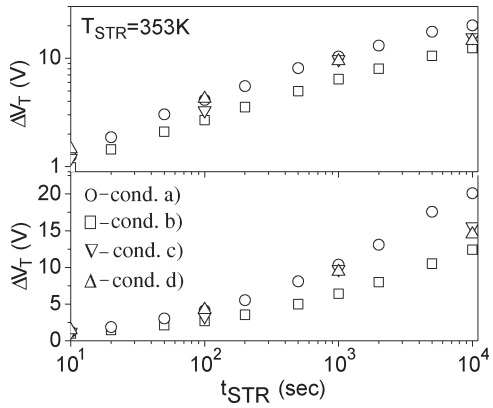

Fig. 6. Variation of ΔV_T with the stress time on both (top) log and (bottom) linear scales, at $T_{\mathrm{STR}} = 353$ K, for the following BTS conditions: (a) $V_{\mathrm{GS}} = V_{\mathrm{DS}} = 40$ V; (b) $V_{\mathrm{GS}} = 40$ V and $V_{\mathrm{DS}} = 0$ V; (c) $V_{\mathrm{GS}} = 40$ V and the drain is floating; and (d) $V_{\mathrm{GD}} = 40$ V and the source is floating.

using the conventional single-step processes, the advanced a-Si:H TFT shows promising electrical performance while having the advantage of a shorter overall deposition time.

B. Bias Instability of the a-Si:H TFT

Fig. 5 (top) shows the evolution of the saturation transfer characteristics with the stress time (t_{STR}) for the BTS condition (a) in the linear scale. The device degradation is defined as the change in the threshold voltage (ΔV_T), i.e.,

$$\Delta V_T = V_T(t = t_{\mathrm{STR}}) - V_T(t = 0). \tag{6}$$

The threshold voltage is extracted from the saturation region transfer characteristic, and the method of extraction is described in the previous section. Each transfer curve in Fig. 5 signifies the electrical performance of the a-Si:H TFT after a given t_{STR}. As stressing time progresses, the curves shift to the right, whereas the slope remains the same. When using the linear fit extraction method described earlier, the field-effect mobility remains the same with increasing t_{STR}; we only need to address the increase in the threshold voltage.

Fig. 6 shows the variations of ΔV_T for the four BTS conditions described above [(a), (b), (c), and (d)] in both log and linear scales. The largest degradation [condition (b)] occurs when a high electric field (1 MV/cm) is set up across the entire gate insulator, assuming that the entire channel area is grounded by the source and drain terminals. TFTs stressed under conditions (c) and (d) have similar ΔV_T compared to condition (b). Although either the source or drain terminal is floating, the potential at the floating terminal should be similar to that at the grounded terminal because the current flow between the two terminals is negligible. This suggests that the electric field profile across the gate insulator for conditions (c) and (d) is similar to that for condition (b), resulting in similar ΔV_T values. The lowest shift occurs in condition (a), although it is the only one with a current flow during electrical stressing. Our BTS experiments confirm the observation made by other groups that a high drain current alone does not necessarily lead to a high threshold voltage shift in an a-Si:H TFT [19], [41]. This agrees with the observation made by Powell *et al.* [19], where they suggest strong field dependence of the trapping mechanism in the a-SiN$_X$:H and near the a-SiN$_X$:H/a-Si:H interface. One theory that explains such observation is that electron hopping at the Fermi level is proportional to the gate-induced electric field [42]. In BTS condition (a), only the source region experiences a high gate electric field; therefore, the majority of electron trapping occurs near the source. In BTS conditions (b), (c), and (d), however, the entire channel region of the TFT experiences a high electric field. Thus, the TFT stressed under these BTS conditions shows larger threshold voltage shifts because the electrons that are accumulated in the entire channel can hop along the Fermi level into the amorphous silicon nitride gate dielectric. This result indicates that the most stable operational region for a TFT is when the gate and drain electrical potentials are identical because the gate-induced electric field near the drain region is minimized. Under such biasing condition, only the source region experiences a high gate-induced electric field. Such region of operation is the saturation region of operation, where $V_{\mathrm{GS}} < V_{\mathrm{DS}} - V_T$.

C. Current Instability of the a-Si:H TFT

The extraction of device degradation for the CTS is the same as for the BTS—using the threshold voltage shift of the saturation transfer characteristics as the parameter to quantify the electrical instability. Furthermore, the TFT transfer characteristics for different t_{STR} values are shown in Fig. 5 (bottom). The ΔV_T plot versus t_{STR} of the a-Si:H TFTs under the CTS is shown in Fig. 7 (symbols). The top portion represents the CTS experiments conducted under the linear region of operation (CTS 1), and the bottom portion represents the saturation region of operation (CTS 2). The TFTs undergoing the CTS suffer larger device degradation when they operate in the linear region than in the saturation region—for example, with 500 nA of stress current, the transistor biased in the CTS 1 condition has ΔV_T of almost 6 V after 10 000 s, whereas the TFT biased in CTS 2 only experienced ΔV_T of less than 1 V for the same T_{STR} and t_{STR}. The transistors' high-temperature electrical stability improves up to a factor of five when changing the biasing condition from CTS 1 to CTS 2. Under the more stable CTS biasing condition, namely, CTS 2, the highest threshold voltage

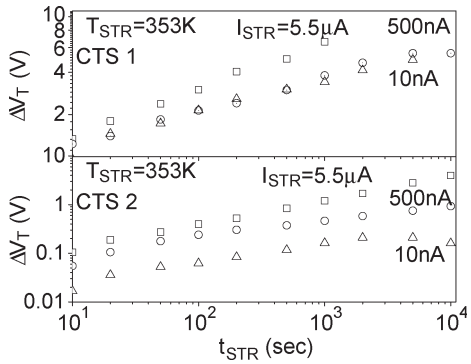

Fig. 7. CTS-induced ΔV_T for the advanced a-Si:H TFTs at a stress temperature of $T_{\rm STR} = 353$ K for (top) $V_{\rm GS} = 20$ V and (bottom) $V_{\rm GS}(t) = V_{\rm DS}(t)$.

shift is less than 4 V when $I_{\rm STR} = 5.5\ \mu$A, $T_{\rm STR} = 353$ K, and $t_{\rm STR} = 10\,000$ s. This trend is consistent with the observation made in the BTS experiments. Changing the biasing condition on a transistor extends its operational lifetime—under CTS 1, a TFT stressed with 5.5 μA of current at 353 K has a threshold voltage shift of 2 V after only 31 s, whereas a TFT experiencing the same thermal ($T_{\rm STR} = 353$ K) and electrical ($I_{\rm STR} = 5.5\ \mu$A) stresses biased in the CTS 2 condition reaches the same level of shift after 2600 s.

Based on the CTS experiments, we can see that the biasing conditions of the gate and the drain are critical for minimizing the threshold voltage shift of the a-Si:H TFT. Two identical TFTs can suffer different threshold voltage shifts while driving the same current if the gate-to-drain electric fields are different. In the case of CTS 1, a large fraction of the gate insulator experiences a high electric field—up to 0.5 MV/cm near the source region and 0.35 MV/cm near the drain region for $I_{\rm STR} = 5.5\ \mu$A; the gate field accelerates electrons into the insulator and causes the formation of trapped charges near the a-Si:H/a-SiN$_X$:H interface. On the contrary, the same TFT undergoing the CTS with the gate and the drain shorted together (CTS 2) experiences much less electrical degradation even if the stress current and the temperature are identical. This is due to a reduction of the electric field across the gate insulator by biasing the gate and the drain at the same potential—for $I_{\rm STR} = 5.5\ \mu$A, the highest value of the gate-induced electric field (0.32 MV/cm) occurs at the source, and no vertical electric field is held at the drain. The calculation of the electric field is done by dividing the gate voltage by the total gate insulator thickness; this calculation assumes that all the applied voltages are dropped across the gate insulator. Under this condition, only electrons that are close to the source get accelerated and injected into the gate insulator as trapped charges that contribute to a positive direction threshold voltage shift. Electrons near the drain region only experience a lateral electric field. Since electron hopping via E_F is gate-field dependent, CTS 2 results in a smaller threshold voltage shift than CTS 1 because 1) field-induced trapping only occurs near the source region instead of the entire channel, and 2) the vertical electric field near the source is reduced by 40%—from 0.5 to 0.32 MV/cm. Under the CTS 2 stressing condition, the maximum threshold voltage shift we observe is less than 4 V when $I_{\rm STR} = 5.5\ \mu$, $T_{\rm STR} = 353$ K, and $t_{\rm STR} = 10\,000$ s.

We have demonstrated that transistors operating in the saturation region suffer less electrical characteristic degradation during the electrical stress due to a reduction of the gate-induced electric field. We would like to emphasize that this reduction physically can translate to decreases in charge trapping, the creation of metastable states, or a combination of both mechanisms that contribute to the threshold voltage instability. This concept is fully applicable to a current-driven AM-OLED circuit—driving TFTs in an AM-OLED should ideally operate in the saturation region because it makes the drain current invariant to the drain voltage and is only controlled by the gate voltage [43].

IV. Impact of the Threshold Voltage Shift on an AM-OLED

In this section, we evaluate the impact of the threshold voltage degradation on the electrical performance of a pixel electrode circuit for an AM-OLED proposed by Lin *et al.* [21], [44]. During the ON-state of the pixel electrode circuit shown in [21, Fig. 1(b)], $V_{\rm SCAN}$ turns on the switching transistors $T1$ and $T2$ to allow the data current $I_{\rm DATA}$ to charge the storage capacitors $C_{\rm ST1}$ and $C_{\rm ST2}$. As the pixel electrode circuit switches from the ON-state to the OFF-state, $V_{\rm SCAN}$ turns $T1$ and $T2$ off, whereas $V_{\rm CTRL}$ turns $T4$ on. Charges stored in $C_{\rm ST1}$ and $C_{\rm ST2}$ during the ON-state remain as $T2$ is turned off. However, $V_{\rm B-ON}$ changes from its ON-state value, as determined by $I_{\rm DATA}$, to its OFF-state value $V_{\rm B-OFF}$ because of the change in the $V_{\rm SCAN}$ value [21], i.e.,

$$V_{\rm B-OFF} = V_{\rm B-ON} - \Delta V_{\rm SCAN} \cdot \frac{C_{\rm ST2}//C_{\rm OV-T2}}{C_{\rm ST1} + C_{\rm ST2}//C_{\rm OV-T2}} = V_{\rm B-ON} - V_{\rm SCALING}. \quad (7)$$

With $V_{\rm B-OFF}$ holding its OFF-state value, it determines the amount of the OLED current $I_{\rm OLED}$ flowing through $T4$, $T3$, and the OLED during the OFF-state of the operation.

The threshold voltage shift compensation takes place because $V_{\rm B-ON}$ is determined by $I_{\rm DATA}$, $\mu_{\rm EFF}$, $C_{\rm INS}$, V_T, W, and L of $T3$; it will automatically adjust with changing the threshold voltage of $T3$ to allow $I_{\rm DATA}$ to flow through. The following equation is modified from (2) and replaced with variables discussed in this section to show the change in $V_{\rm B-ON}$ with the threshold voltage [21]:

$$\left[\frac{I_{\rm DATA}}{\frac{W_3}{2L_3}\mu_{\rm EFF}C_{\rm INS}}\right]^{1/2} + (V_T + \Delta V_T) = V_{\rm B-ON}. \quad (8)$$

The symbols V_T and ΔV_T stand for the initial threshold voltage value and the change in the threshold voltage, respectively. The value in the parentheses represents the total threshold voltage of $T3$. It is clear that, although $V_{\rm B-ON}$ is set by $I_{\rm DATA}$, it linearly increases with ΔV_T to achieve the compensation effect to the threshold voltage instability. Therefore, ideally, any threshold voltage shift of $T3$ will be fully compensated by $I_{\rm DATA}$ by increasing the voltage at the V_B and V_A nodes, and the OFF-state OLED current will not be affected by the

threshold voltage shift of $T3$, as demonstrated by the following equations [21]:

$$I_{\mathrm{OLED}} = \frac{W_3}{2L_3}\mu_{\mathrm{EFF}}C_{\mathrm{INS}}\left(V_{\mathrm{B-OFF}} - (V_T + \Delta V_T)\right)^2 \tag{9}$$

$$I_{\mathrm{OLED}} = \frac{W_3}{2L_3}\mu_{\mathrm{EFF}}C_{\mathrm{INS}} \times \left(V_{\mathrm{B-ON}} - V_{\mathrm{SCALING}} - (V_T + \Delta V_T)\right)^2 \tag{10}$$

$$I_{\mathrm{OLED}} = \frac{W_3}{2L_3}\mu_{\mathrm{EFF}}C_{\mathrm{INS}} \times \left(\left(\frac{I_{\mathrm{DATA}}}{\frac{W_3}{2L_3}\mu_{\mathrm{EFF}}C_{\mathrm{INS}}}\right)^{1/2} + (V_T + \Delta V_T) - V_{\mathrm{SCALING}} - (V_T + \Delta V_T)\right)^2 \tag{11}$$

$$I_{\mathrm{OLED}} = \frac{W_3}{2L_3}\mu_{\mathrm{EFF}}C_{\mathrm{INS}} \times \left(\left(\frac{I_{\mathrm{DATA}}}{\frac{W_3}{2L_3}\mu_{\mathrm{EFF}}C_{\mathrm{INS}}}\right)^{1/2} - V_{\mathrm{SCALING}}\right)^2. \tag{12}$$

We can see from the above OLED current equation that the threshold voltage shift has no effect on the OLED current in the ideal case. However, another factor could influence I_{OLED}—the threshold voltage shift of $T4$ along with the channel length modulation effect of $T3$. Our analysis will focus on ΔV_T of $T4$ during the OFF-state, with the assumption that $T3$'s ΔV_T can be fully compensated.

Although $T4$ is defined as a switching transistor, it experiences the same amount of current flow as the driving transistor ($T3$) throughout the OFF-state. During the ON-state of the circuit, $T4$ provides the data current to the OLED; a positive threshold voltage shift of $T4$ results in a decrease in the OLED current during the OFF-state. This is caused by the effective increase in the channel resistance associated with the threshold voltage degradation of $T4$ and the channel length modulation of $T3$ [21]. As $T4$'s channel resistance increases, a larger voltage drops across its source and drain, which leads to a smaller voltage drop across the source and the drain of $T3$. This causes the $T3$ drain current to decrease because of the channel length modulation factor, along with the OLED luminance. Quantitatively, this decrease in the OLED current can be computed by simultaneously solving the OLED current equations flowing through $T3$ and $T4$. We developed the following equations to describe the relation between ΔV_T and ΔI_{OLED} caused by $T4$'s electrical instability (ΔV_{T4}) and $T3$'s channel length modulation factor λ:

$$I_{\mathrm{OLED}} = \frac{W_3}{2L_3}\mu_{\mathrm{EFF}}C_{\mathrm{INS}}\left(V'_{\mathrm{B-OFF}} - V_T\right)^2(1 + \lambda V'_A) \tag{13}$$

$$I_{\mathrm{OLED}} = \frac{W_4}{2L_4}\mu_{\mathrm{EFF}}C_{\mathrm{INS}}\left((V'_{\mathrm{CTRL}} - V'_A) - (V_T + \Delta V_{T4})\right)^2. \tag{14}$$

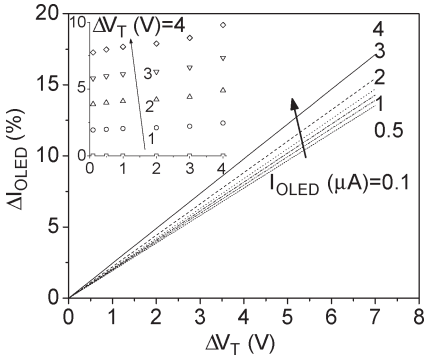

Fig. 8. Simulated OLED current decrease with a $T4$ threshold voltage shift and a $T3$ channel length modulation factor of 0.05 V^{-1}. (inset) ΔI_{OLED} with I_{OLED} ranging from 0.1 to 4 μA for ΔV_T from 0 to 4 V.

We simplified the mathematics by setting the voltage across the OLED (V_{OLED}) as the reference—$V'_{\mathrm{CTRL}} = V_{\mathrm{CTRL}} - V_{\mathrm{OLED}}$, $V'_A = V_A - V_{\mathrm{OLED}}$, and $V'_{\mathrm{B-OFF}} = V_{\mathrm{B-OFF}} - V_{\mathrm{OLED}}$. The channel length modulation factor is set at 0.05 V^{-1}, and we assume that $T3$ and $T4$ have identical transistor geometric and electrical parameters. By setting the two OLED equations equal to each other, we can solve the value of V'_A using the following quadratic formula:

$$V'^2_A - V'_A\left[2\left(V'_{\mathrm{CTRL}} - (V_T + \Delta V_{T4})\right) + \lambda\left(V'_{\mathrm{B-OFF}} - V_T\right)^2\right] + \left[\left(V'_{\mathrm{CTRL}} - (V_T + \Delta V_{T4})\right)^2 - \left(V'_{\mathrm{B-OFF}} - V_T\right)^2\right] = 0 \tag{15}$$

$$V'_A = -B \pm \sqrt{\frac{B^2 - 4AC}{2A}} \tag{16}$$

where $A = 1$, $B = [2(V'_{\mathrm{SCAN}} - (V_T + \Delta V_{T4})) + \lambda(V'_{\mathrm{B-OFF}} - V_T)^2]$, and $C = [(V'_{\mathrm{SCAN}} - (V_T + \Delta V_{T4}))^2 - (V'_{\mathrm{B-OFF}} - V_T)^2]$. It is important to clarify that we only account for the channel length modulation of $T3$ and not $T4$. Moreover, we assume the ideal case where charges stored on C_{ST1}, C_{ST2}, and the gate of $T3$ remain constant throughout the OFF-state, with negligible dielectric leakage and charge injection from $T2$. Based on (13) and (14), we plot the simulated result for the OLED current decrease (ΔI_{OLED}), as defined in [21, eq. (5)], with respect to the threshold voltage shift of $T4$ for I_{OLED} values ranging from 0.1 to 4 μA (Fig. 8); this range is selected to reflect the current values that are necessary to drive an OLED in XGA displays at various gray scales [21]. At a given I_{OLED}, there is linear dependence between the OLED current decrease and $T4$'s threshold voltage increase—a ΔV_T increase from 1 to 7 V causes ΔI_{OLED} to increase from 2.5% to 17.1% for $I_{\mathrm{OLED}} = 4$ μA. Moreover, for constant ΔV_{T4}, ΔI_{OLED} increases with I_{OLED} as seen in the inset of Fig. 8, where we plot ΔI_{OLED} versus I_{OLED} for ΔV_T ranging from 1 to 4 V. The OLED current degradation occurs in the presence of ΔV_T regardless of the magnitude of the actual OLED current level. Based on our CTS experimental result, we see that after applying I_{STR} of 5.5 μA for 1000 s at 353 K, if $T4$ is biased in the CTS 2 mode, ΔI_{OLED} will be 2.9% when driving I_{OLED}

of 4 μA. This OLED degradation increases to 16.2% if the biasing scheme for $T4$ is CTS 1. This drastic change suggests that all transistors in a pixel electrode circuit should be biased in the CTS 2 scheme to prolong the operation of the entire display panel.

V. Conclusion

We have shown that the advanced amorphous silicon TFT deposited at a high rate has promising electrical performance, with acceptable field-effect mobility and a low drain current activation energy. Our a-Si:H TFT, which has a relatively small W/L ratio, can withstand up to 5.5 μA of the current stress for 10 000 s at 353 K and still suffers ΔV_T of less than 4 V. The transistors operating in the saturation region undergo a less threshold voltage shift during electrical stressing than the same transistors operating in the linear region. This trend was observed in both CTS and BTS experiments. For the AM-OLED pixel electrode circuit studied in this paper, the application of 5.5 μA of the continuous stress current for 1000 s at 353 K causes a threshold voltage shift of 1.2 V, which translates to a 2.9% decrease for an OLED current of 4 μA. Changing the operating condition of a-Si:H from the linear to the saturation region in a pixel electrode circuit alone can achieve an improvement of a factor of five in the circuit electrical stability. This technique can improve the stability of the TFT regardless of its electrical performance and quality because it does not require making any fundamental changes to the TFT. For engineers designing the circuit for an AM-OLED, we recommend that all driving transistors be maintained in the CTS 2 condition at all times to minimize the electrical degradation. Also, it is recommended that the a-Si:H TFT's ΔV_T be less than 3 V during the operation of the AM-OLEDs. Such ΔV_T is expected to produce ΔI_{OLED} of 5.8% for $I_{\mathrm{OLED}} = 0.1$ μA to 7.3% for $I_{\mathrm{OLED}} = 4$ μA, which is acceptable for many display applications.

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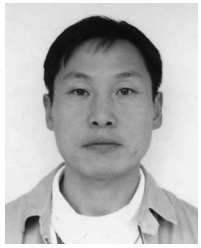

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